(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 658 994 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94119837.6**

(51) Int. Cl.[6]: **H04L 7/00**

(22) Date of filing: **15.12.94**

(30) Priority: **16.12.93 IT TO930956**

(43) Date of publication of application:
21.06.95 Bulletin 95/25

(84) Designated Contracting States:
DE FR GB IT NL SE

(71) Applicant: **CSELT Centro Studi e Laboratori Telecomunicazioni S.p.A.**
Via Guglielmo Reiss Romoli, 274
I-10148 Turin (IT)

(72) Inventor: **Gambini, Piero**
Via Sineo, 16
Torino (IT)
Inventor: **Vezzoni, Emilio**
Via Carisio, 21
Torino (IT)

(74) Representative: **Riederer Freiherr von Paar zu Schönau, Anton et al**
Lederer, Keller & Riederer,
Postfach 26 64
D-84010 Landshut (DE)

(54) Method of and device for the fine synchronization of ATM cells in optical ATM nodes.

(57) Within an optical ATM node, an ATM cell to be synchronized is sent into a segment of pre-determined length of an optical fibre with a high time dispersion (FD), after having been associated, in a tunable wavelength converter (CL), to an optical carrier with a wavelength that is different from that with which the cell itself was received and such that, as an effect of the transit the fiber (FD), the cell reaches the input side of a switching element (Em1...Emh) of the node (NC) at a predetermined instant.

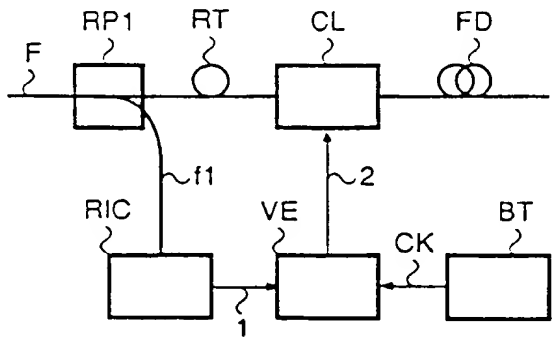

Fig. 2

EP 0 658 994 A1

The invention described herein relates to switching nodes of fast cell switching networks (or ATM - Asynchronous Transfer Mode - networks) in optical technology, and more specifically it concerns a method and device for the fine synchronization of the cells in one of such nodes.

The ATM technique is taking on a growing importance for the transport and switching of digital flows at very high speed, such as those present in wide band integrated service digital networks. In this technique, the information associated with the various services is organized into contiguous packets of fixed length (about 400 bits), called "cells", formed by an information field and a header field (tag) that carries service information, including the information necessary for the routing through the network.

In an ATM network, the switching nodes must carry out two fundamental tasks: routing the cells (thus performing a spatial switching function), and avoid possible conflict situations, which occur when several cells entering the node simultaneously from different inputs have to be routed toward the same output (thus, the node performs a memorization function). In order to satisfy the requirements for bit rate and bandwidth of modern integrated services networks, ATM switching nodes based on optical techniques have been proposed. There, both routing and memorization are performed by means of optical devices: in this way, it has been possible to operate at very high bit rates, of the order of various Gbit/s.

An example of a node of this type is described, for instance, in European patent application EP-A-0 411 562 of the same applicant.

In a communication system based on the ATM technique, the cells containing information may be emitted by the various transmitting stations at random times. In the optical systems proposed so far, there is the need for a synchronization of the cells arriving at the various inputs of a node, so as to facilitate its operation. In a large optical switching node, comprising a multi-stage network, there may be a further synchronization need, due to the uncertainty about the length of the optical paths that the cells travel through in the node. In the first case, the cell synchronization system must be able to recover time shifts of ± half a cell, whereas in the second case the time shift to be recovered may be of much smaller proportions, in the order of a few nanoseconds.

The synchronization of the ATM cells arriving at the different inputs of a single-stage optical switching node is described in European patent application EP-A 0 411 562 mentioned above. The time realignment is performed by acting on signals converted into electrical form, within the devices performing the tag processing necessary for routing. The possibility to operate directly on optical signals is also suggested.

The purpose of the invention is to provide a method and a device for the fine synchronization of ATM cells, which are aimed at compensating delays due to possible differences in optical paths within the node, by exploiting the dependence of dispersion in an optical fiber on wavelength.

According to the invention, a method is provided in which the cell to be realigned is sent into a segment of predetermined length of optical fiber with high time dispersion, after having been associated to a re-phasing optical carrier of such a wavelength that, as a result of the transit through the fiber, the cell reaches the input of a subsequent switching element of the node at a predetermined instant, and in which the beginning of the cell to be realigned is recognized, the time delay between the beginning of the cell and a reference instant is evaluated, and an error signal representative of the entity of this delay is generated, the error signal causing the transfer of the cell from an original carrier, to which the cell to be realigned is associated, to the re-phasing carrier.

A system arranged to impose a continuously variable delay on an electrical signal by exploiting the dependence of the dispersion in an optical fiber on wavelength is described in the paper "Continuously variable true-time-delay modulator" presented by J. L. Dexter *et at.* at the OFC/IOOC '93 conference, San José (Ca., USA), 21-26 February 1993, paper ThC6. A signal, representative of the desired variable delay, modulates the wavelength of a tunable optical source, and the optical carrier generated by the source is then amplitude modulated by the electrical signal in an electro-optical modulator and sent into a segment of optical fiber. Given the wavelength variation, the signal exits the fiber with a variable delay. The delayed signal is then converted again into electrical form. The system is not aimed at compensating a delay with respect to a reference, and thus it is not applicable for the synchronization of ATM cells.

According to the invention, a device is also provided for carrying out the method, in which the cell to be realigned is sent into a segment of predetermined length of an optical fiber with high chromatic dispersion, after having been associated to a re-phasing optical carrier having such a wavelength that, as a result of the transit along the fiber, the cell reaches the input of a switching element of the node at a predetermined instant. The device comprises: means for extracting a fraction of the optical signal associated with the cell to be realigned; means for recognizing the beginning of the cell, by utilizing the said fraction of optical signal, and for generating a signal representing the occurred recognition; means for receiving the sig-

nal representing the occurred recognition of the beginning of the cell, for comparing it with a signal representing a reference instant, and for generating an error signal indicative of the entity of the delay between the two signals; and a tunable wavelength converter, driven by the error signal, to transfer the cell to be realigned from an original carrier, to which the cell arriving to the device is associated, to the re-phasing carrier.

For the sake of further clarification, reference is made to the enclosed drawing, where:

- figure 1 is a block diagram of a switching node utilizing the invention;
- figure 2 is a block diagram of the device according to the invention;
- figure 3 is a circuit diagram of some of the blocks in figure 2; and
- figure 4 is a time diagram of some signals utilized to evaluate the error.

In figure 1, NC is the connection network of an optical ATM switching node with n inputs and n outputs connected to respective optical fibers Fe1...Fen, Fu1...Fun. The node comprises, in the most general case, m stages composed of elements E11... E1h... Em1... Emh that, purely as an example, are represented as elements with two inputs and two outputs. The structure of the node and of the switching elements has no interest for the purposes of the present invention. In general, at any rate, current ATM optical nodes present an optical connection network and an electrical control structure; this latter is not indicated in the figure because it is not influenced by the invention. Input fibers Fe1...Fen are associated to devices SY1...SYn which perform, for all ATM flows present over their respective fiber, any necessary processing of the call identification and the phase realignment of the cells needed to compensate the random emission times on the part of the respective sources and possible random fluctuations of the propagation times. Devices SY can be, for instance, of the type described in the aforementioned European patent application. Fine synchronization devices SF1...SFn are associated to the inputs of the switching elements of the stages of node NC subsequent to the first, so as to compensate for any possible differences in the cell optical paths between one stage and the next, which differences may give rise to differences in propagation time in the order of a few nanosecond.

Devices SF, which constitute the subject matter of the invention, exploit the dependence of dispersion in an optical fiber on wavelength. More particularly, devices SF evaluate the delay of the beginning of the cell to be realigned with respect to a time reference and send the cell to a segment of high dispersion fiber after having associated the cell with an optical carrier that is different from the one with which the cell has been received and is chosen in such a way that, given the length of the fiber segment, the cell appears at the output of the latter at the desired instant. Devices such as SF may also be associated to devices SY to refine, if need be, the phase realignment performed by them.

The block diagram of a device SF is represented in more detail in Figure 2, where the thick lines indicate the path of optical signals and the thin lines indicate the path of electrical signals. A power divider RP1 extracts a fraction of the power of the optical signal at wavelength $\lambda 1$ associated to a cell present on fiber F and sends that fraction to a recognizer of the beginning of the cell, RIC, through a fiber segment f1. Recognizer RIC provides a signal indicative of the occurred recognition to a device VE for evaluating the time error. VE operates a comparison between the instant of recognition of the beginning of the cell and a time reference instant (communicated by the time base BT of the node) and generates an electrical error signal representative of the entity of the delay between the beginning of the cell and the reference. The remaining part of the optical power is sent by RP1, through an optical delay element RT which has the task of compensating the processing times in RIC and VE, to a tunable wavelength converter CL whose output is connected to a segment of high dispersion optical fiber FD, connected to the input of the switching element interested in node NC. Converter CL also receives the error signal generated by VE and, on the basis of that signal brings wavelength $\lambda 1$ of the cell to a value $\lambda 2$ such that, taking into account the dispersion characteristics and the length of fiber segment FD, the cell arrives at the input of the subsequent switching element at a predetermined instant.

Devices carrying out the functions of CL are well known in the art. An example is described in the paper "High performance optical wavelength shifter", by B. Glance *et al.*, Electronics Letter, Vol. 28, No. 18, pages 1714-1715.

The use of a segment of high dispersion fiber allows keeping the length of the segment limited, and therefore achieving time realignment without introducing large delays.

Figure 3 illustrates a possible embodiment of blocks RIC and VE. The structure described for block RIC is based on the hypothesis that the cell header includes an initial word (of 4 bits in the example shown) of predetermined configuration. Block RIC includes a second power divider RP2 which shares the power present on f_1 among four different outputs connected to respective optical fiber segments $f_2...f_5$ (or in general, among as many paths as are the bits in the initial word of the cell). The four fiber segments have such a length

that the signals exit f_3, f_4, f_5 with a delay that exceeds respectively by 1, 2, or 3 bit times the delay introduced by f_2. The fiber segments $f_2...f_5$ thus constitute an optical series-to-parallel converter SP. The four bits in the initial word are detected in parallel in as many detectors represented within the block RIV and, after being converted into logic signals by threshold decision circuits DS, are provided to a comparator COM that compares the configuration present at the output of RIV with a configuration established for the initial word, read in a memory ME. In case of positive outcome of the comparison, comparator COM emits on wire 1 a signal of the appropriate logic level (e.g., at level 1).

In the error evaluation circuit VE a set-reset flip-flop FF has the set input connected with wire 1 and output $\overline{Q}$ connected to an input of an AND gate AN whose other input receives a time reference signal CK1 provided by BT. The signal exiting AN, which is a pulse of a duration proportional to the delay of the pulse over wire 1 with respect to reference CK1, is provided to an integrator IN, which generates a voltage signal whose amplitude is proportional to the duration of the impulse coming from AN. The integrated signal is provided to a sample-and-hold circuit CT, controlled by a sampling pulse CK2 emitted by BT at an instant that is certainly subsequent to the end of the pulse emitted by AN (e.g. after a maximum delay allowed for the cell has elapsed). Integrator IN is reset by a signal CK3 emitted by BT in an instant subsequent to CK2. Circuit CT generates a signal of stable level that is provided to an equalization circuit EQ that has the task of compensating the non-linear characteristics of the source in wavelength converter CL (figure 2). Therefore the error signal controlling the wavelength conversion in CL is present on output 2 of EQ.

The various signals intervening in circuit VE are represented also in figure 4, where lines 1, $\overline{Q}$, AN, IN, CT indicate respectively the signals present on wire 1, on the output of FF and on the output of circuits AN, IN, CT.

It is evident that what is described above is provided solely as a non-limiting example and that variants and modifications are possible without departing from the scope of the invention. For example, in the recognizer of the cell beginning it would be possible to perform the detection directly on the serial signal present on f_1 and to carry out the series-to-parallel conversion on the eletrical signals; however, the series-to-parallel conversion performed optically allows elimination of the bandwidth and attenuation problems which would be encountered when acting on electrical signals. Moreover, though optical fibers have been mentioned, it is clear that the components of the device could utilize integrated optics guides. Still further, the signal on wire 1 could be issued after COM has recognized the initial word for a predetermined number of times (for instance 3 or 4) at intervals equal to the cell period.

Claims

1. Method of fine time realignment of ATM cells in an optical ATM switching node, in which a cell to be realigned is sent over a segment of predetermined length of an optical fiber with a high time dispersion, after having been associated to a rephasing optical carrier at such a wavelength that, as an effect ot the fiber dispersion, the cell reaches the input of a subsequent switching element (Em1...Emh) of the node (NC) in a predetermined instant, characterized in that the beginning of the cell to be realigned is recognized, the time offset between the beginning of the cell and a reference instant is evaluated, and an error signal representative of the entity of that offset is generated, to command the transfer of the cell from an original carrier, to which the cell to be realigned is associated, to the rephasing carrier.

2. Method as claimed in claim 1, for the time realignment of cells presenting a predetermined initial bit configuration, characterized in that the recognition of the beginning of the cell comprises the following operations:
   - series-to-parallel conversion of the optical bits of the cell to be realigned, with a degree of parallelism equal to the number of bits in the said initial configuration;
   - detection and conversion into logic signals of each group of optical bits resulting from the series-to-parallel conversion;
   - comparison of each group of logic signals with the said initial configuration; and
   - generation of a signal of predetermined logic level when the comparison has a positive outcome.

3. Method as claimed in claim 1 or 2, characterized in that, for the generation of the error signal, a signal of a duration proportional to the delay between the recognition instant and the reference instant is obtained from the signal indicative of the recognition of the beginning of the cell; such signal is integrated to obtain a signal with an amplitude proportional to the delay, and the integrated signal is sampled to obtain a signal of stable level.

4. Method as claimed in claim 3, characterized in that the signal resulting from the sampling is equalized to compensate any possible non-linearities of means performing the wavelength conversion operation.

5. Device for the fine time realignment of ATM cells in an optical ATM switching node, where a cell to be realigned is sent into a segment of an optical fiber of predetermined length (FD) with high time dispersion, after having been associated to a rephasing optical carrier of such a wavelength that, as an effect of the transit along the fiber, the cell reaches the input of a subsequent switching element (Em1...Emh) of the node (NC) at a predetermined instant, characterized in that it comprises:
   - means (RP1) for extracting a fraction of the optical signal associated to the cell to be realigned;
   - means (RIC) for recognizing the beginning of a cell, by utilizing the said fraction of the optical signal, and for generating a signal representative of the occurred recognition;
   - means (VE) for receiving and comparing the signal representative of the occurred recognition of the beginning of the cell with a signal representative of a reference instant, and for generating an error signal indicative of the entity of the delay between the two signals;
   - a tunable wavelength converter (CL), driven by the said error signal, to transfer the cell to be realigned from an original carrier, to which the cell received by the device is associated, to the rephasing carrier.

6. Device as claimed in claim 5, for the time realignment of cells presenting a predetermined initial bit configuration, characterized in that the means for recognizing the beginning of the cell include:
   - a series-to-parallel converter (SP) of the optical bits of the cell to be realigned, the converter having as many outputs as are the bits in said initial configuration;
   - detection means (RIV) for converting into logic electrical signals each group of optical bits exiting the series-parallel converter (SP);
   - a comparison logic network (COM) for comparing each group of logic signals with said initial configuration and generating a signal at predetermined logic level when the comparison gives a positive outcome.

7. Device as claimed in claim 5 or 6, characterized in that the means (VE) for the generation of the error signal include:
   - a bistable device (FF), which is activated by the signal at predetermined logic level emitted by said comparison logic (COM) and is reset at the end of the cell;
   - a two-input logic gate (AN), which receives at a first input the time reference signal (CK1) and at a second input the output signal of said bistable device (FF) and generates a pulse of a duration that is proportional to the delay of the output signal of the bistable device (FF) with respect to the reference signal;
   - an integrator (IN) for converting the output signal of the logic gate (AN) into a signal with an amplitude that is proportional to the delay;
   - a sample-and-hold circuit (CT) that samples the signal leaving the integrator (IN), and generates a signal at a stable level that constitutes the error signal.

8. Device as claimed in claim 7, characterized in that it comprises an equalization circuit (EQ) that receives the error signal from the sample-and-hold circuit (CT) and provides it to the tunable wavelength converter (CL) after having compensated any non-linearities of the sources in converter (CL).

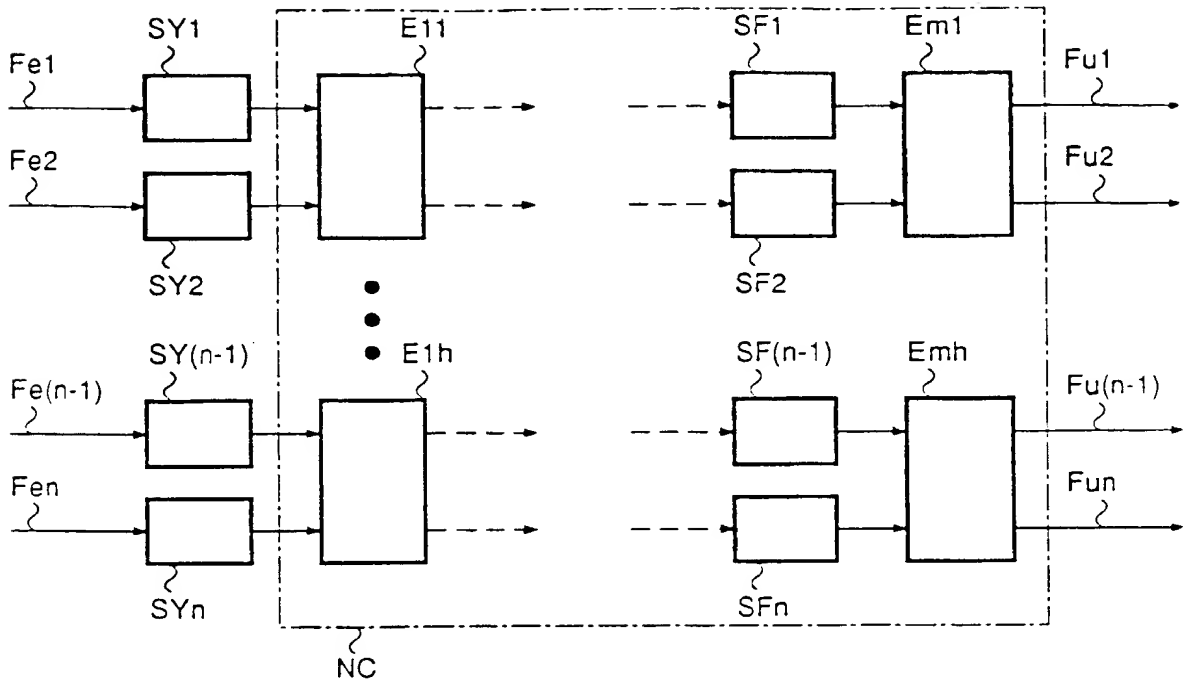

Fig. 1

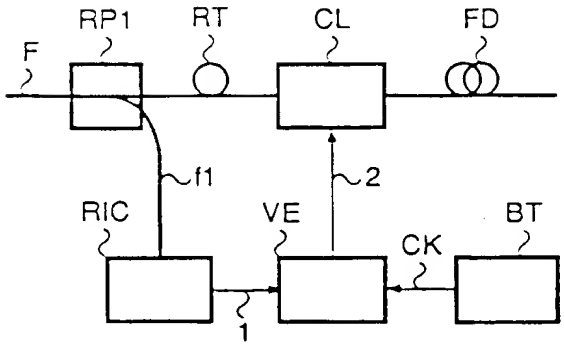

Fig. 2

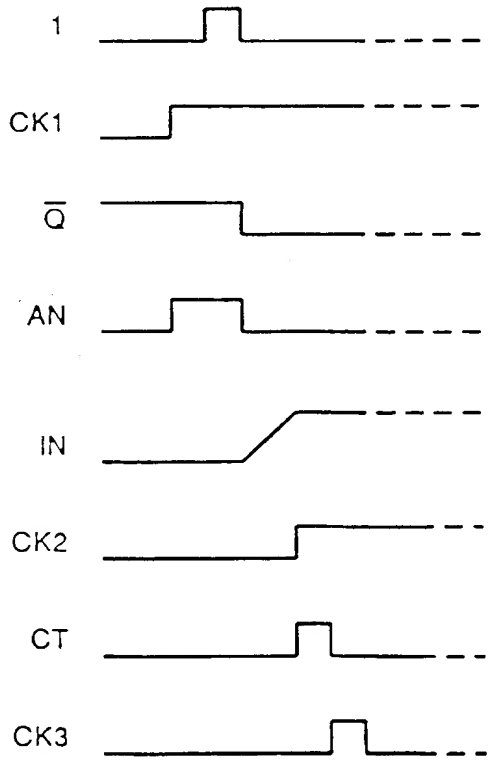

Fig. 4

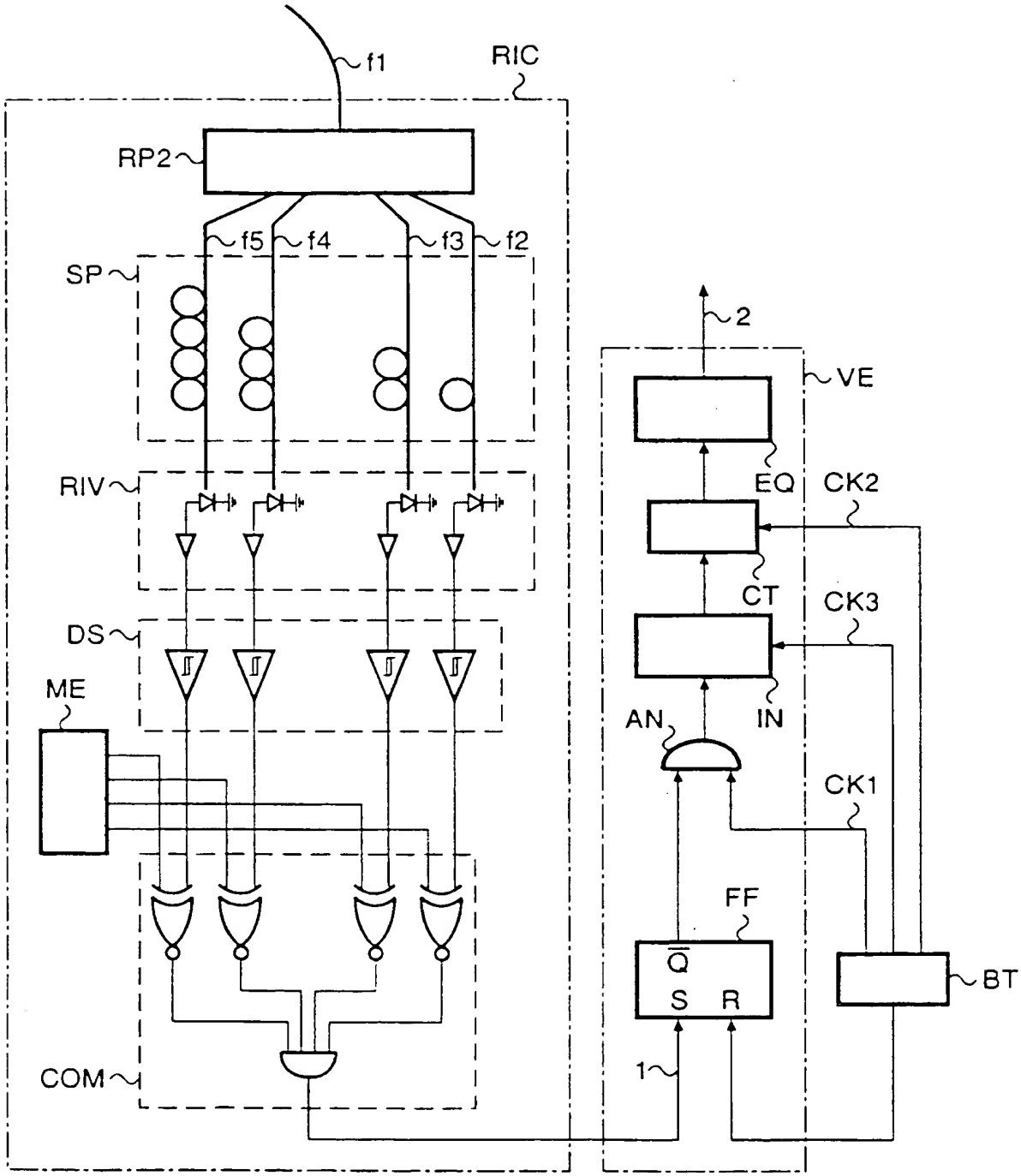

Fig. 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 9837

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	GLOBECOM '90: IEEE GLOBAL TELECOMMUNICATIONS CONFERENCE AND EXHIBITION. 'COMMUNICATIONS: CONNECTING THE FUTURE' , SAN DIEGO, CA, USA, 2-5 DEC. 1990, vol.1 pages 206 - 210 BALLANCE J W ; LEE R F ; ROGERS P H ; HALLS M F 'A B-ISDN local distribution system based on a passive optical network.' * page 207, right column, line 24 - line 37 * * page 208, left column, line 27 - line 35 * ---	1-8	H04L7/00
D,A	OFC/IOOC, 26 February 1993, SAN JOSé (CA, USA) pages 172 - 173 J.L. DEXTER ET AL. 'CONTINUOUSLY VARIABLE TRUE-TIME-DELAY MODULATOR' * page 173, left column, line 7 - line 10 * ---	1,3-5	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04L
A	INTERNATIONAL SWITCHING SYMPOSIUM 1992. 'DIVERSIFICATION AND INTEGRATION OF NETWORKS AND SWITCHING TECHNOLOGIES TOWARDS THE 21ST CENTURY' PROCEEDINGS, YOKOHAMA, JAPAN, 25-30 OCT. 1992 pages 412 - 416 BARNSLEY P E ; WICKES H J ; WICKENS G E 'Switching in future ultra high capacity all optical networks' * page 413, right column, line 48 - line 55 * * page 414, left column, line 2 - line 24 * -----	1,5	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 March 1995	Canali, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)